New developments in neutron counting chains for safeguards

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Abstract:

Standard neutron counting systems in nuclear safeguards typically use a thermal neutron absorber material in gas proportional counters embedded in a neutron moderator block, and surrounding the central sample cavity. Multiple detector tubes are normally connected to one electronics chain composed of a pre-amplifier, an amplifier, a single channel analyser and a digital signal mixer summing signals from multiple chains to produce a single pulse train representing the neutron detection events. This has typically been the design compromise considering factors such as the dead-time of the detection system, the reliability of the electronics, complexity and cost.

In this paper we describe the ongoing developments at JRC for modernizing the entire electronics chain, including all the individual components mentioned above as well as the digital signal analyser. A key element of this work concerns an in-house designed digitizer board capable of processing pre-amplifier outputs to identify neutron detection events. The board has multiple analogue inputs, a multichannel ADC, pulse processing in FPGA hardware and output of timestamps of neutron detection events. The benefits from this work are expected to be a reduced pulse processing time in the electronics, better pulse pair resolution, the elimination of the physical signal analyser and better systems diagnostics.

The new electronics developments are being assembled and tested in the JRC reference passive neutron counter, and will be ready for demonstration in the coming year. The reference counter is a cylindrical well-counter incorporating 126 ^{3}He neutron detector tubes.

Keywords: NDA; neutron counter; digitiser; list-mode; safeguards

1. Introduction

Several non-destructive techniques (NDA) and devices for safeguards using passive or active neutron measurement methods have been developed and tested at the Joint Research Centre (JRC) over decades.

Traditionally a neutron measurement chain consists of analogue and digital components: a detector with high voltage bias supply, a preamplifier, an amplifier/shaper circuit and, finally, a digital discriminator. Modern neutron detection systems apply many ^{3}He or BF_3 gas proportional counters in order to increase the neutron detection probability and to reduce the paralysing, or updating, dead-time effects.

A necessary requirement for systems of multiple detection chains is that the resulting digital signal lines must be summed to produce one signal pulse train for the analysis, without suffering loss of real signals and without causing false spurious signals. An analogue electronics chain performs rather well when only few parallel measurement chains are used, i.e. when several detectors grouped together within a moderator block are connected to a single measurement chain.

High efficiency neutron well-counters often use dozens of such measurement chains. Particular care must be observed when manufacturing such devices in order to eliminate internally or externally generated electromagnetic noise. Such precautions can include using proper filters on the high voltage rail, using multi-layer printed circuit boards (PCBs), separating analogue and digital ground planes, avoiding creating inductive paths that may amplify ground bounces [8], etc.

Such passive neutron counting systems currently operated at JRC include, for example, the Drum Monitor, the Boron-Based Neutron Coincidence counter (BBNCC), and neutron slab counters, applying 28, 6 and 1 analogue chains respectively. These systems output Transistor-to-Transistor Logic (TTL) pulse signals, representing neutron detection events, to be counted by means of standard signal analysers such as multichannel scalers (MCS) or shift registers (SH/R) commonly used in multiplicity analysis. The analysers are routinely used with standardised measurement software, for example for nuclear inspectors.

Most often, TTL signal outputs are used to maintain compatibility with existing analysers. An important part of the analogue electronics is the discriminator that filters out signals not originating from neutron detections but from other effects, for example gamma-ray background, and false bursts caused by electromagnetic noise. The discriminator level is set carefully to avoid eliminating real neutron signals, and not to trigger multiple output signals from a single analogue pulse. Correctly setting the discriminator can, in part,

eliminate gamma background and spikes of noise caused for example, by TTL ground bounces whose noise contribution to the analogue signal can increase significantly when multiple parallel measurement chains are in use. Each analogue pulse crossing the discrimination level triggers the output of a logical pulse for further processing.

Modern technologies offer alternative approaches to the solution of problems encountered in a standard analogue chain. For example, implementing measurement components using field programmable gate arrays (FPGA), and using low-voltage differential signal standards (M-LVDS) to propagate signals within the neutron counter [1]. In case a TTL output signal is needed to maintain compatibility with external instrumentation, a digital pulse can easily be produced as output.

The text below describes such techniques and components, we have implemented so far, together with other efforts currently under development in order to process neutron detection events using more modern digital techniques.

We use a Moving Window Deconvolution (MWD) algorithm [2] to process a signal in an entirely digital fashion using appropriate digital filters implemented in FPGA state-of-the-art technology. Another effort concerns implementing a novel low-noise charge pre-amplifier to be implemented eventually with every single ^{3}He tube, thus avoiding connecting several tubes to a single pre-amplifier. This will reduce the updating dead-time of the combined system. An analogue pulse shaper will no longer be used, but will be substituted by a digital filter featuring a comparable or possibly shorter shaping time. A final advantage of the digital pulse processing chain is expected simply from all data being transmitted via high-speed optical USB3.0 link. Avoiding the usage of multiple 50-Ohm coaxial cables will simplify the implementation of the overall system, as expected for example in a planned high-efficiency counter using 126 ^{3}He tubes. Multiplicity analysis and/or multichannel scalers are easily integrated inside the FPGA fabric.

Applying a pre-amplifier to each detector tube makes the individual tubes independent rather than integrated into the shared detection system. This fact greatly facilitates the sharing of ^{3}He proportional counters between neutron well-counters, thus avoiding the purchase of many ^{3}He tubes with a single usage in mind.

1.1 Digital techniques

The main advantages proposed in this paper for changing to digital processing techniques in neutron NDA instrumentation for safeguards are as follows:

1. elimination of noise spikes returning to the pre-amplifier input and generated by TTL digital output signals from another electronics chain. Low-voltage differential signal lines (M-LVDS Standard) can be an alternative to single ended TTL logic;
2. reduction of the dead-time, and possibly improved detection of pile-up pulses;
3. recording of both the timestamp and the energy information of a radiation detection event. The added energy information can help discriminate high-energy events, for example caused by cosmic radiation or unwanted ionisation;
4. if compatibility with existing instrumentation needs to be maintained, a TTL output pulse can be generated at the same time the timestamp is computed.

1.2 Time digitisers for neutron counting applications in safeguards

Neutron coincidence counting is the reference NDA technique used in nuclear safeguards to measure the mass of nuclear material in samples. Most neutron counting systems are based on the original shift register technology. The analogue signal from the ^{3}He tubes is processed by a charge amplifier/discriminator producing a train of TTL digital pulses that are fed into an electronics unit which records frequency distributions of neutron detections in short time intervals. In recent years many research laboratories have instead produced the frequency distributions based on software-based analysis of timestamps of detection events. For this purpose, so-called list-mode acquisition devices produce the list of timestamps. Standard laptops or desktop computers (PCs) are often seen that utilise external acquisition boards based on FPGA technology, providing a timestamp for every incoming digital signal. The acquisition can be performed at high data rates utilising the ubiquitous Universal Serial Buses (USB 2.0 or USB 3.0) for transfers to the host PC with typical data throughput in the order of 40 MB/s and 300 MB/s, respectively.

The timestamps of a given measurement are often saved to storage devices. This has the advantage that measurement data can be reanalysed with different parameter values, such as gate pre-delay and gate width. Other useful diagnostics information such as die-away time, dead-time, performance of individual electronics chains, and eventually electronics noise can be filtered from the original data stream. The diagnostics information can be extracted from this stored data, or even in real-time under certain circumstances.

At JRC, two models of the Time Digitizers for Safeguards (models TDS8 and TDS32) were developed with the timestamp features described above. The TDS8 and TDS32 are shown in Figure 1. The devices record the arrival time of digital pulses with a 10 ns resolution, and feature 8 or 32 input channels respectively. Also, the channel number is recorded for each event. Data are transferred to a host PC over USB 2.0 or USB 3.0 data links. The data throughputs are 38 MB/s and 300 MB/s respectively. The devices are housed in a small extruded aluminium enclosure and in

a standard 19-inch rack 1U enclosure respectively. Other features include powering over USB (TDS8) and front panel Light Emitting Diodes (LED) for each input line, allowing the user to observe the incoming pulses on individual channels (TDS32). A signal output on the rear panel is the sum of all input channels, and can be routed, for example, to a standard shift register analyser for comparison and/or test purposes. In both devices the recorded events are written into a dual-port memory block in the FPGA. Dual-port memories guarantee independence between the processes of writing and reading data simultaneously. Decoupling the data producer and data consumer allows a simpler but very efficient hardware/firmware design.

A state machine, evolving through several states (IDLE, WRITE _ START _ RECORD, WAIT FOR PULSE, WRITE _ PULSE _ EVENT, WRITE _ ROLLOVER _ EVENT and WRITE _ STOP _ RECORD) transfers into dual port memory the time of arrival of the TTL or LVTLL signal on individual input channels.

The TDS8 uses a timestamp of 32 bits, so a roll-over event happens every 42.795 s, while the TDS32 uses timestamps of 29 bits, giving roll-over events every (2^{29}-1 × 10ns) equals 5.185 s. The generation of a roll-over event allows arrival times to be measured in absolute time.

A Wishbone System-on-Chip (SoC) bus [3] makes data available to the host PC using a buffered USB transmission.

The usefulness of list-mode devices such as the TDS8 and TDS32 is shown in Table 1 and Table 2, where data records from a neutron background measurement are examined. The examples show bursts of noise in a 2 us coincidence window either from a single channel or on multiple channels.

Table 1 shows the timestamps of TTL events on channel No 4 within several hundred nanoseconds. Knowing that events from neutron detections cannot appear so close on a single channel, the last two events are removed in the diagnostic analysis.

Table 2 gives an example of a burst of 10 false signals likely caused by sporadic electromagnetic noise. Such events happen occasionally in large detection systems. Note, for example, that the second timestamp represents three signals observed on different channels in the same 10 ns clock step.

A simple OR circuit performs well for background measurements and other low count rate applications. At high count rates, however, summing of OR-gated signals

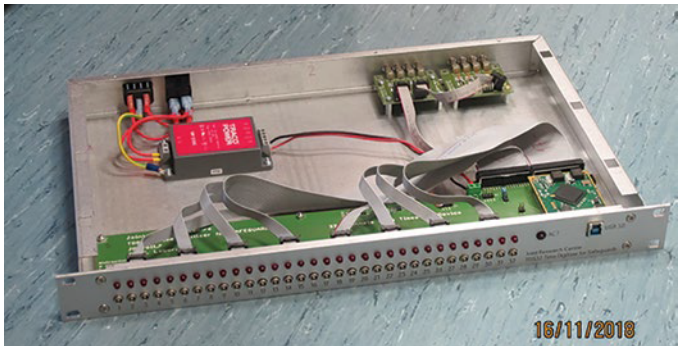

Figure 1: The TDS8 and TDS32 list-mode devices developed at JRC, one with 8 front panel inputs, the other with 32.

Channel number	Bit encoded channels	Timestamp
CH4	0b00000100	0[d] 0[h] 8[min] 25[s] 704[ms] 116[us] 540[ns]
CH4	0b00000100	0[d] 0[h] 8[min] 25[s] 704[ms] 117[us] 360[ns]
CH4	0b00000100	0[d] 0[h] 8[min] 25[s] 704[ms] 118[us] 140[ns]

Table 1: Example of noise detected on one channel (from TDS8).

Channel number	Bit encoded channels	Timestamp
CH15	0b00000000000000000100000000000000	0[d] 7[h] 29[min] 32[s] 866[ms] 820[us] 100[ns]
CH14,CH16,CH18	0b00000000000001010100000000000000	0[d] 7[h] 29[min] 32[s] 866[ms] 820[us] 160[ns]
CH17	0b00000000000001000000000000000000	0[d] 7[h] 29[min] 32[s] 866[ms] 820[us] 220[ns]
CH11	0b00000000000000000000010000000000	0[d] 7[h] 29[min] 32[s] 866[ms] 820[us] 280[ns]
CH19,20	0b00000000000011000000000000000000	0[d] 7[h] 29[min] 32[s] 866[ms] 820[us] 520[ns]
CH12	0b00000000000000000001000000000000	0[d] 7[h] 29[min] 32[s] 866[ms] 820[us] 600[ns]
CH3	0b00000000000000000000000000000100	0[d] 7[h] 29[min] 32[s] 866[ms] 820[us] 720[ns]
CH9	0b00000000000000000000000100000000	0[d] 7[h] 29[min] 32[s] 866[ms] 822[us] 40[ns]

Table 2: Example of a burst of electromagnetic noise recorded by TDS32 from a multichannel passive neutron counting system.

results in coincident or near-coincident events being lost in the process. The number of lost signals increases with the count rate.

For high count rate purposes, a digital mixer has been added to the TDS32 device. In this context we define a mixer as a circuitry with a de-randomiser on each input line and a buffer for recording the content of all input lines. A synchronous priority encoder is then used to output the buffer content on a single output line without the loss of the incoming signals. An output clock of 12.5 MHz has been adopted in order to output signals with a width of 40 ns. In this way the minimum distance between signals remains 80 ns. Because only the presence of signals is needed at this stage, a proper first-in-first-out (FIFO) is not necessary. Only read and write event-pointers are needed to advance the 'virtual FIFO' and to record the signal arrivals. An output signal is produced when the read pointer reaches the write-pointer in accordance with the following rules:

1. the read-pointer must be less than or equal to the write pointer, except for the condition outlined by the second rule. This means that a read operation normally follows a write operation as soon as the read has been enabled, i.e. when the priority encoder is freed from processing signals;
2. the read-pointer can only be greater than the write-pointer when a roll-over of pointers has occurred due to the limited size of the buffer. In this case the virtual FIFO must be sequentially emptied;
3. the virtual FIFO must not be read faster than the 12.5 MHz output clock rate. This condition is necessary to avoid the output of two signals instead of one while the priority encoder is busy.

Modulo 32 (5-bit) Gray code counters have been implemented but used as modulo 16 (4-bit) counters, the most significant bit being used to indicate pointer 'wrap-arounds'. For this reason, only 16 FIFO slots are available on each individual line. Gray code counters exhibit an improved read-out error code with respect to binary counters, because only 1-bit transitions can happen between adjacent words. Bursts of electrical noise, such as the ones detected by the post-processing analysis of the pulse train (Tables 1 and 2), can also be eliminated by including filters in the mixer FPGA fabric. A simple inhibit gate on each individual line can eliminate for example situations depicted in Table 1, but not in Table 2.

This kind of real-time filtering should be performed only at low count rates or in background measurements in order to avoid removing real signals.

1.3 Signal digitiser for safeguards

At JRC we are currently in the process of developing an analogue signal digitiser to substitute the standard signal amplifier used in neutron counting instrumentation for safeguards. The signal digitiser will have eight analogue signal input lines intended for pre-amplifier signals from gas proportional counters. The main benefits of this prototype compared to the standard analogue front-end electronics are expected to be:

— reduced updating dead-time on each signal line;
— improved discrimination of pile-up events.

The digitiser will process the analogue charge pre-amplifier output with the characteristic long exponential decay by means of a Moving Window Deconvolution (MWD) and a 'feature extraction algorithm' (FEA). The algorithms are currently being tested in our laboratory. The hardware is expected to be operational by the end of 2019.

A larger version featuring up to 128 channels to be housed inside a detector head is the final goal. In this way a single optical USB cable from the detector eliminates the complex wirings of multiple coaxial cables normally interfacing a neutron detector head to a signal analyser.

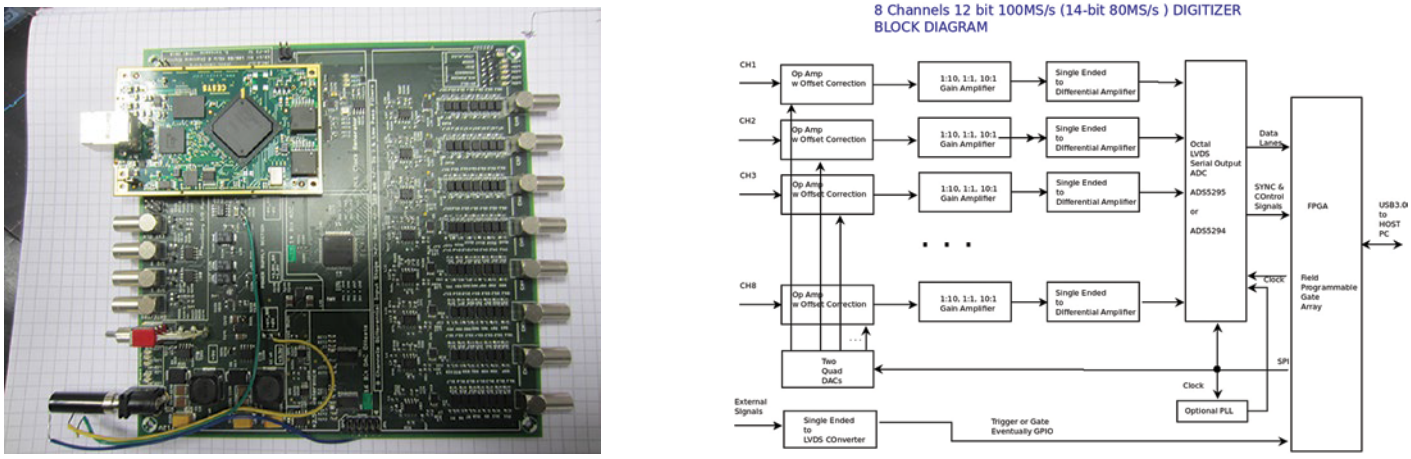

Figure 2: The prototype signal digitiser board and corresponding block diagram.

The hardware is enclosed in an extruded aluminium box (170 mm × 163 mm × 51.5 mm) with the following characteristics:

- sampling rate up to 100 MS/s (ADS5295) and 80 MS/s (ADS5294), depending on chipset;
- 12-bit (ADS5295) or 14-bit (ADS5294) resolution;
- 8 channels, DC coupled, fixed input impedance: moderately high impedance (kΩ) or 50Ω;
- trigger options: internal (software or driven by channel(s) criteria) or external (TTL logic levels);
- gate: external TTL signal;
- clock options: internal or external;
- digitally controlled gain, in principle settable independently for each channel (the current version uses the same gain for all channels to simplify the board design on a 4 layers PCB);
- input sensitivity covers the range from ± 50 mV (100 mVpp), ± 500 mV (1 Vpp), ± 5 V (10 Vpp) for ADC full scale;
- 50 (40) MHz analogue bandwidth, anti-aliasing LC filter included. Coefficients for low-pass filters can also be uploaded to the ADC registers.

2. Digital filter using Moving Window Deconvolution and feature extraction algorithm

The MWD algorithm, see Georgiev, Gast and Lieder [2], consists in a technique to determine a value proportional to the step amplitude of an exponential decaying signal (the output of a charge pre-amplifier) by looking at the sequence of values of the signal at successive time intervals. The values evidently contain an indication of the step value A assumed at t = 0. In the continuous time domain, an exponential signal is defined as:

$$y(t) = \begin{cases} Ae^{\frac{-t}{\tau}} & t \geqslant 0 \\ 0 & t < 0 \end{cases} \quad (1)$$

To determine the step amplitude (A), we define a function $f(t) = A$.

A term *y(t)* is added and subtracted:

$$f(t) = y(t) + A - y(t) \quad (2)$$

Then inserting the definition of the exponentially decaying function, the equation reads:

$$f(t) = y(t) + A\left(1 - e^{\frac{-t}{\tau}}\right) \quad (3)$$

By applying the fundamental theorem of integral calculus and using a variable substitution $u = \frac{t}{\tau}$, because

$$\tau \int_0^t e^{-u} du = -\tau e^{-u} \left[\begin{matrix} t \\ 0 \end{matrix} \right] = \tau \left(1 - e^{\left(\frac{-t}{\tau}\right)}\right) \quad (4)$$

we get:

$$f(t) = y(t) + \frac{1}{\tau} \int_0^t y(u) du \quad (5)$$

The sum can be extended to $-\infty$ because the signal is a null function for t < 0.

In the time domain this corresponds to a step function, i.e. the response of an ideal integrator.

To avoid the saturation of a real pre-amplifier, a continuous discharge is applied by a resistor in parallel to the integrating capacitor, so that the exponential response of the real

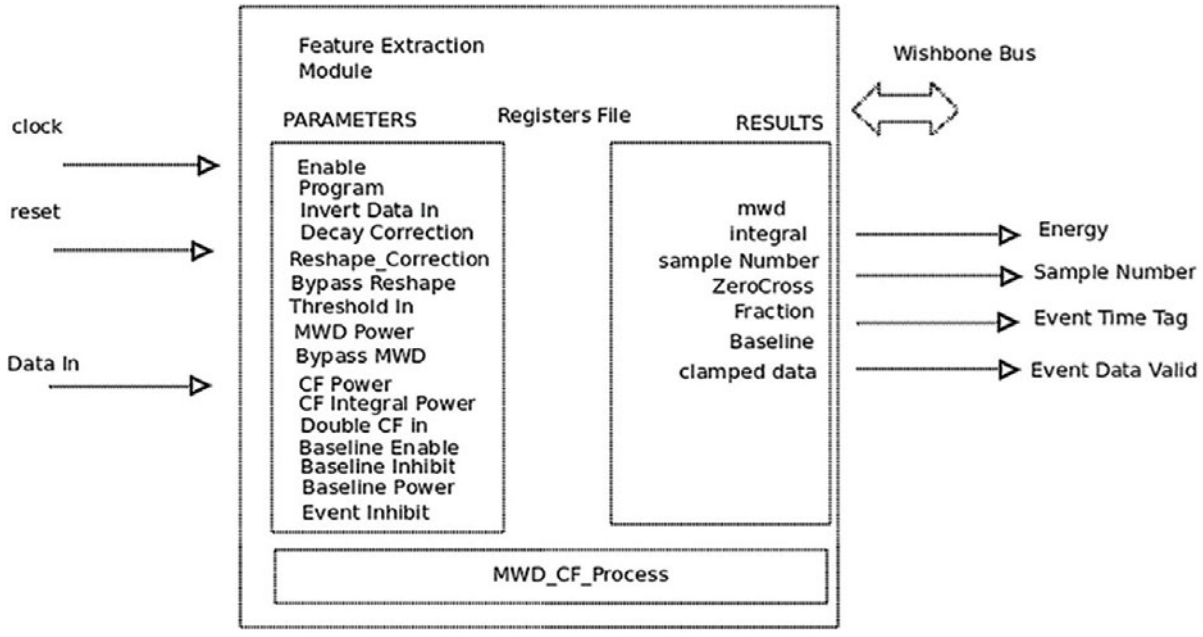

Figure 3: Block diagram in VHDL.

filter is deconvoluted to a step function. In the discrete time domain the integral becomes a sum, also extensible to –∞:

$$A(n) = x(n) + \frac{\Delta}{\tau}\sum_{k=0}^{n-1} x(k) \quad where\ \Delta = \frac{1}{sampling_{rate}} \tag{6}$$

which can also be expressed as a recursion:

$$A(n) = x(n) - \left(1 - \left(\frac{1}{\tau}\right)\right) x(n-1) + A(n-1) \tag{7}$$

Equation 5 is differentiated (in discrete time) because we are interested only in the amplitude step of the signal from the radiation detector, we get:

$$MWD(n) = A(n) - A(n-M) = x(n) - x(n-M) + \frac{\Delta}{\tau}\sum_{k=n-M}^{n-1} x(k) \tag{8}$$

The MWD can be seen as a composition of two elementary blocks: Delay and Subtract (DS), and Moving Average (MA). The DS block takes the amplitude difference at two sampling points which are M sampling intervals apart $y[n] = (x[n] - x[n\text{-}M])$. M is the MWD differentiation filter length. The value of M can be taken as an integer power-of-two in order to easily implement a fast binary division.

2.1 Algorithm implementation

The block diagram of the algorithm as implemented in Very High Speed Integrated Circuits Hardware Description Language (VHDL) code is presented in Figure 3.

The top level block of the MWD filter dialogues with the external word using a Wishbone bus interface [3]. Several registers are available to the user in order to store parameters and constant values for controlling the algorithm. The module outputs are:

- a timestamp indicating when step value A is recognised;
- the corresponding energy (step height);
- an indication of the validity of the data recorded.

The main registers to control the behaviour of the algorithm are:

- decay and reshape correction;
- MWD power (of 2) to give a length (M);
- cross fraction power (division by ¼ or ½) and cross fraction integral power (of 2) length of pipeline;
- baseline power (of 2) so pipeline length;
- baseline inhibit and enable bits;
- event detect inhibit or enable;
- threshold input.

Details of the top-level diagram are given in Figure 4.

The ADC input data, or an inverted value representation, become the input of the programmable MWD module, which can optionally be bypassed. The data can become an input for a shaper module, which may also be bypassed. Following the MWD and shaper blocks, a further, more complex features extraction block follows in Figure 5. Implementing a MWD, consisting of a DS block and an MA block, is an easy task. The features extraction module, however, is not easily implemented. The latter module has been edited and adapted from a remarkable open source code [4-7].

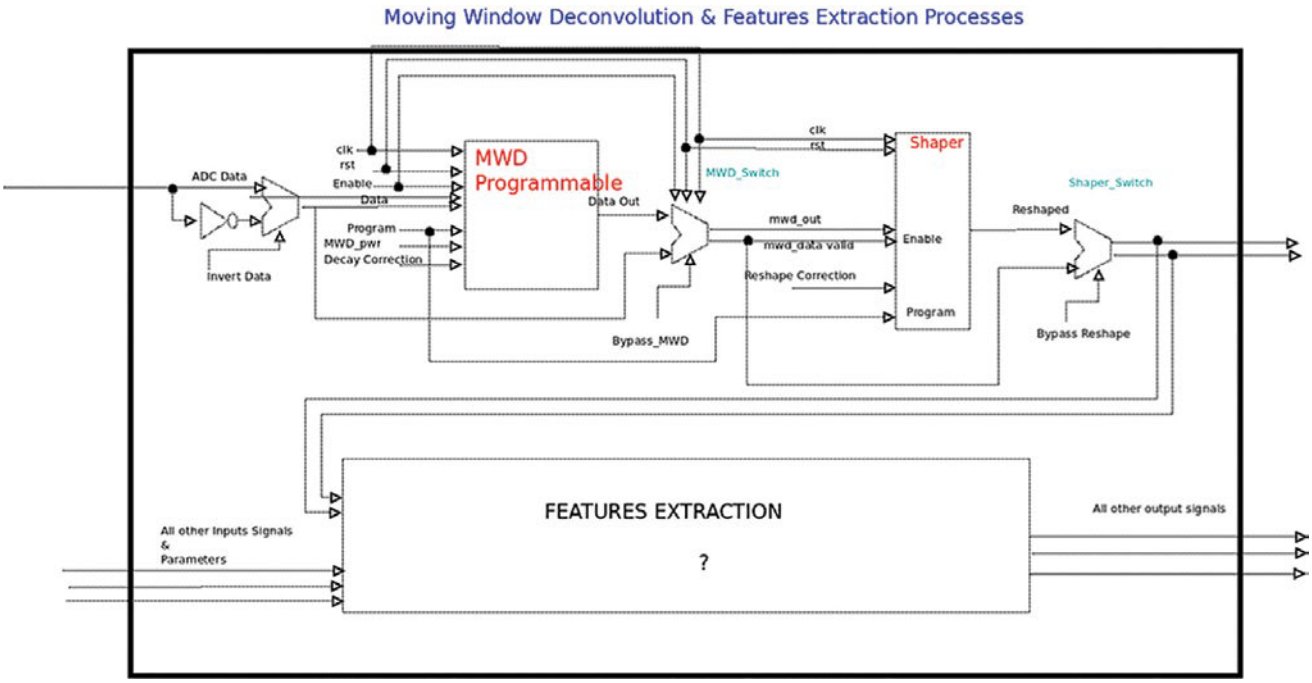

Figure 4: MWD and shaper block diagram.

The MWD logic consists of the moving sum and difference blocks. Fixed point arithmetic operations can be performed easily. However, the normalisation constant $\frac{\Delta}{\tau}$, expressed in units of the ADC sampling period T = 10 ns, is a real number (<1). A typical value is 1/14000 for the Cremat CR110 preamplifier decay constant of 140 µs. In order to make the FPGA implementation of the MWD filter algorithm possible, the normalisation constant is multiplied by an arbitrarily large power-of-two value, and after the multiplication operation the result is divided by the same factor.

2.1.1 Moving Sum or Moving Average (MA)

The MA entity is a basic building block for the MWD, and in general also for FEA. The block is composed of an accumulator register, an adder/subtractor and a delay line. The accumulator contains the sum of the delay-line elements. Each value coming out of the delay line is subtracted from the accumulator. After an initial delay, an averaged value is output at each clock-tick (10ns). It is straightforward to divide (shift right operation) by N if the delay line length (N) is a power of two.

2.1.2 The Features Extraction Algorithm (FEA)

A clamped data signal is obtained from the signal coming out of the previous MWD block and from the signal baseline information, which must be taken into account and subtracted from the input data. Of course, the baseline computation must be disabled during the energy pulse duration interval, otherwise a false value for the baseline would be obtained. In order to compute the energy and timestamp information of step value A, a trigger signal must be determined at the same time.

The features extraction module (Figure 5) contains several blocks which compute different information more or less simultaneously using delayed pipelines, just to get information at a later time after other events have been already detected. In this way the algorithms can be executed in parallel, and global information can be figured out after a delay when a final trigger signal is generated. The algorithm can be run continuously, and is triggerless because the trigger is extracted from incoming data.

A constant-fraction discrimination (CFD) module is used as a preferred choice with respect to the simpler leading-edge discriminator. The CFD entity is implemented by subtracting a delayed copy of the clamped signal, which has been scaled (values are divided by two or four for the sake of simplicity and implementation). The obtained CFD signal has a zero-crossing timing independent of the shape and rise time of the clamped signal. After detection of the zero-crossing a trigger is sent to the event detection module.

An event is detected when an area of the pulse is above the set threshold. The area is computed by means of a trapezoidal filter: another MA module which computes

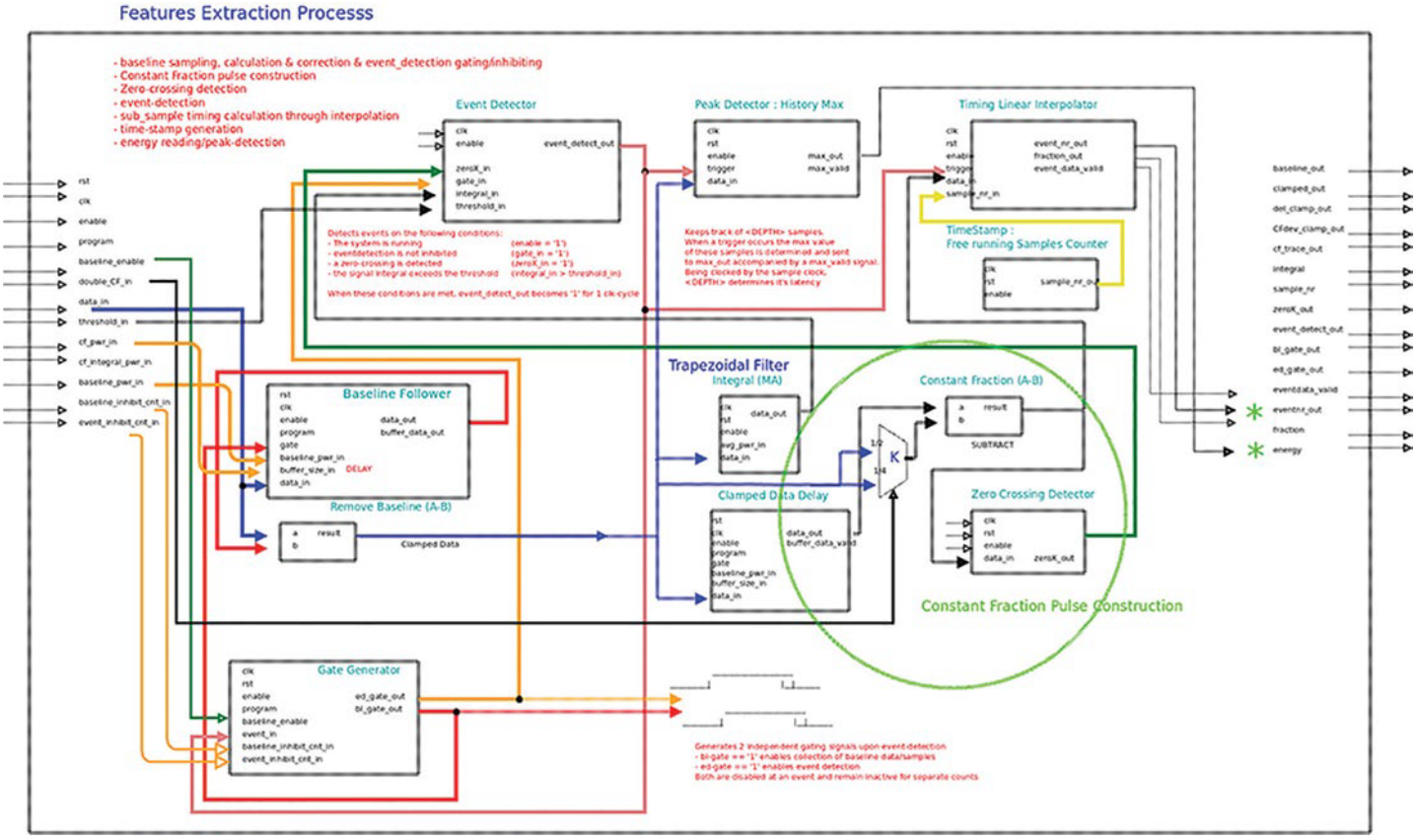

Figure 5: Feature extraction module.

averaged values of the flat top portion of the pulse (as seen in Figure 8). In order to detect the highest pulse level, which is contaminated by noise, a pulse detector is implemented by collecting a limited history of input signals. A timestamp is generated by means of a free running counter, and read upon arrival of the trigger signal. A linear interpolation is then used to determine a less arbitrary and more precise timestamp value. The zero-crossing indication is obtained by a simple algorithm which looks at a sequence of consecutive 'one negative and two positive' values. The time information is between two samples. A linear interpolation of four, eight or more interpolated points can give an even better approximated value.

Parametric values are set up by the user by means of several registers (see Figure 3) in order to fine-tune the behaviour and performance of the algorithm.

2.1.3 Simulations

Figures 6 to 8 below are the results of simulations performed using an open-source hardware description language simulator. The analogue signals are a representation of digital values which, if represented only as numerical values, would have been less expressive of the dynamics of the signals.

The results of the MWD and the FEA are shown below.

Figure 6 shows an input signal which is a superposition of the exponential decaying waveform with a 140 us decay time (simulated pre-amplifier pulse). After the third step the noise level has been increased on purpose to generate a false detection of a timestamp and a corresponding energy value.

After having changed the threshold parameter (Figure 7), the false pulse in Figure 6 has been discarded. This means that tuning the digital algorithm can be as simple and effective as an analogue threshold discrimination circuit.

In Figure 8 a series of nearby pile-up events have been simulated. Pulses were correctly discriminated by the MWD FEA; timestamp and energy information have been generated.

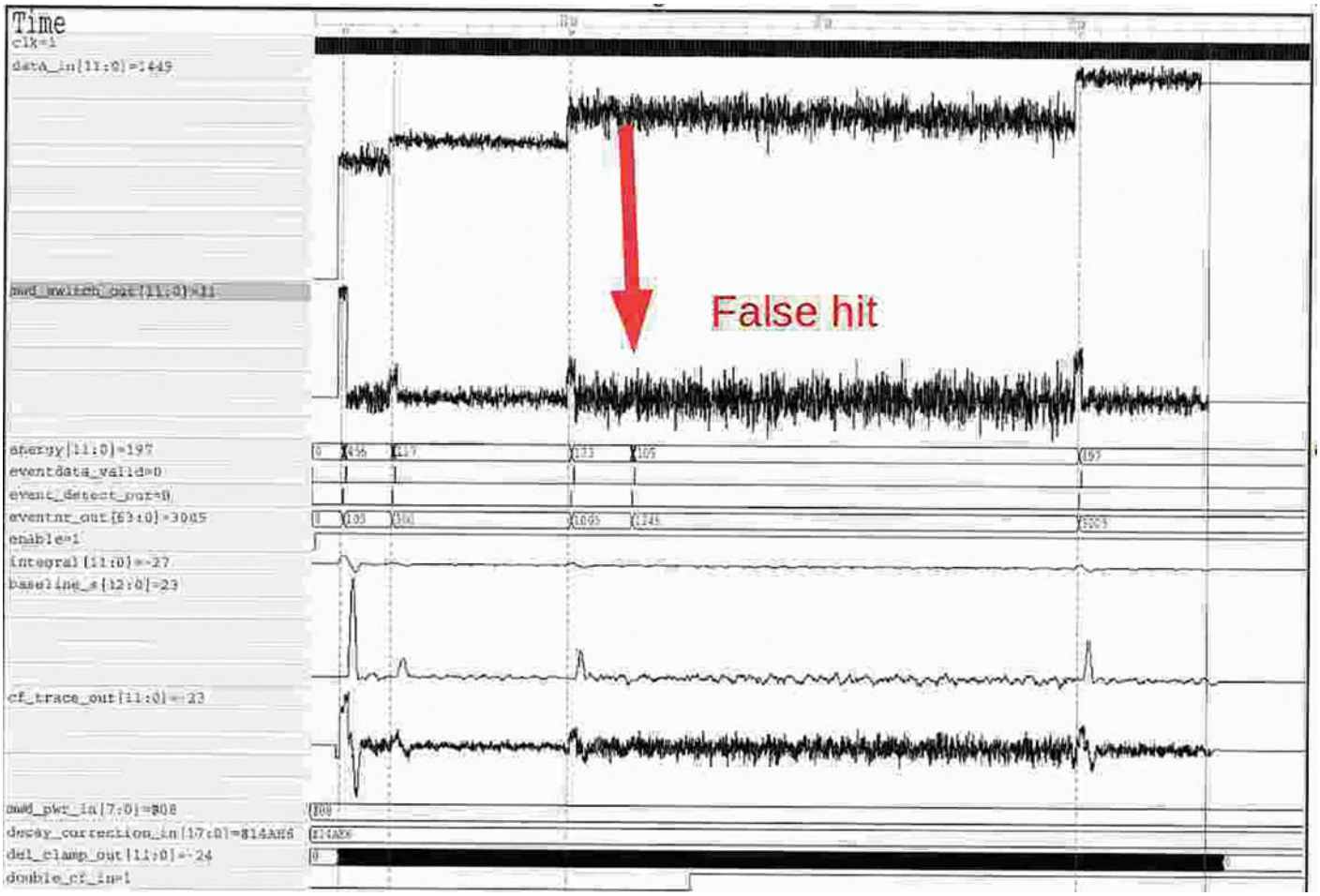

Figure 6: Simulation result No 1.

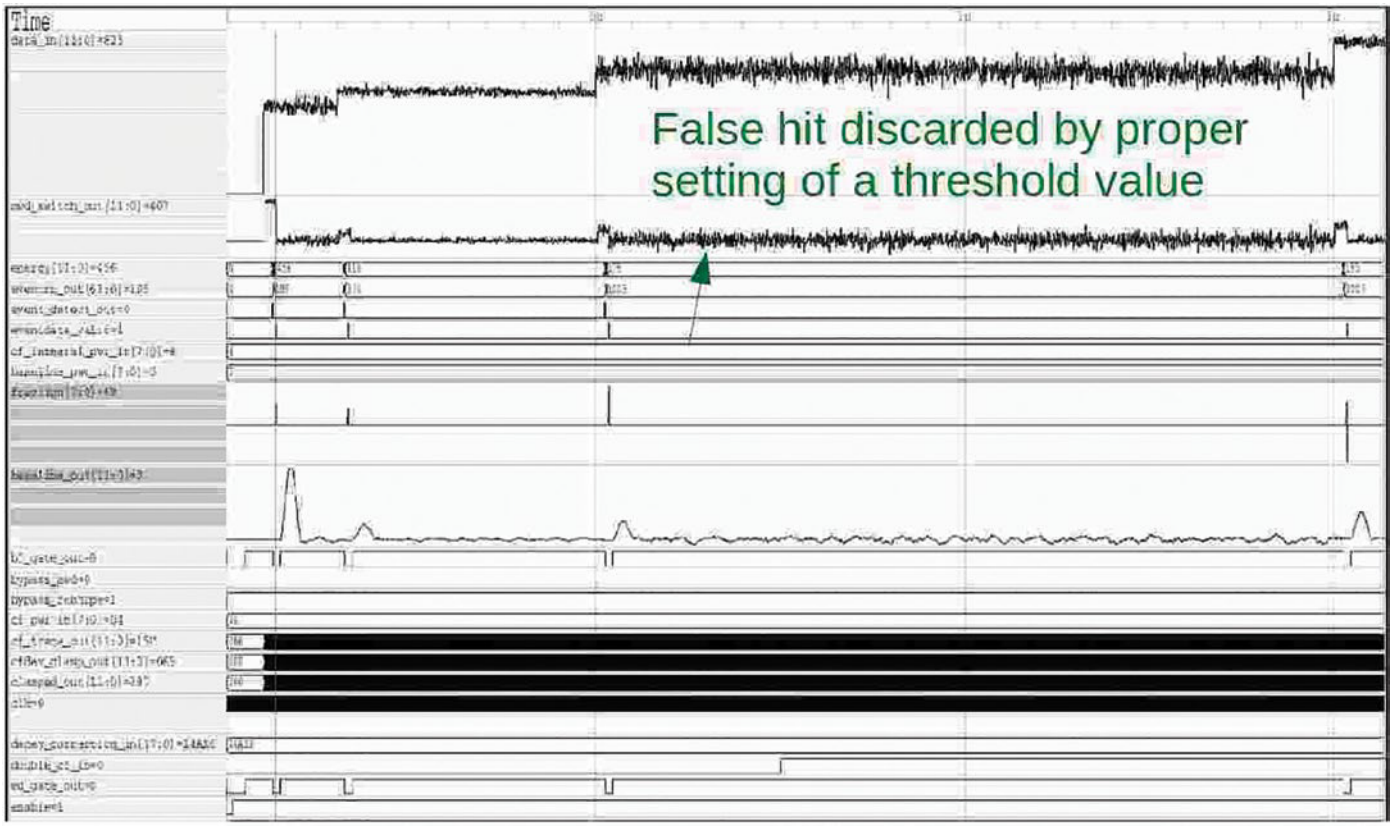

Figure 7: Simulation result No 2.

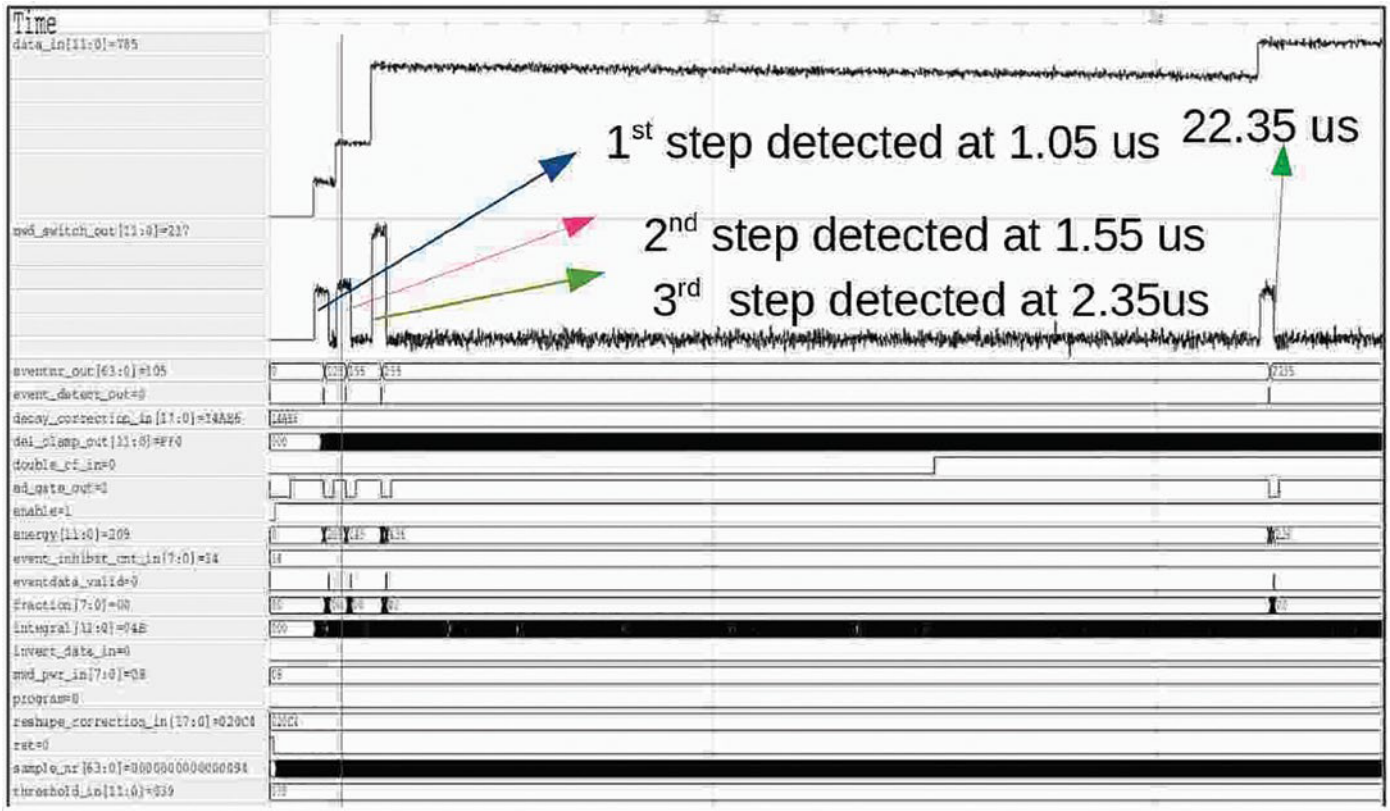

Figure 8: Simulation result No 3.

3. Conclusion

At JRC we are working to improve the electronics chain in neutron counting systems for safeguards. This concerns all the steps from the charge collection pre-amplifier connected to neutron sensitive gas proportional counters to the measured frequency distributions of neutron detection events, as used typically in well-counters for neutron multiplicity counting.

We have presented elements of noise suppression methods used in the development of new pre-amplifiers/amplifier circuits. Also, the new list-mode devices developed at JRC to substitute the standard shift register analysers have been presented, and the data elaboration and diagnostics possible in these devices have been discussed. The main focus, however, was on the ongoing development of digitiser circuits we propose for replacing the traditional signal amplifier and digital signal formation following a neutron-detection event. The advantages of the digital approach are expected to be, first of all, better dead-time performance and pile-up rejection, but also much improved system diagnostics and lower costs. Tests are ongoing on a prototype digitiser board with eight input lines. The promising simulations show the feasibility of implementation, what is basically a digital filter, with potential for the substitution of the widely used analogue methods for neutron-pulse processing in safeguards.

An added advantage of the digital approach derives from the entire signal processing being completely parallelised starting from the single ^{3}He detector tube until the final step of data analysis. This offers the possibility that individual ^{3}He detectors can be moved between detector heads without affecting the electronics design, provided that the neutron-detection heads are purposely designed for easy removal of the tubes. A better utilisation of the ^{3}He tubes in this fashion could alleviate the present shortage of ^{3}He.

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